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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/654,177	09/03/2003	Ian P. Shaeffer	10002500-2	4331

7590 09/15/2005

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EXAMINER	
JOHNSON, JONATHAN J	

ART UNIT	PAPER NUMBER
1725	

DATE MAILED: 09/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/654,177	SHAEFFER ET AL.	
	Examiner	Art Unit	
	Jonathan Johnson	1725	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-23 and 26-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-23 and 26-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9-3-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

The examiner withdraws the restriction requirement made on 8-4-05.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14-23, 26-29 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,320,139 (Byle). Byle teaches providing a printed circuit board defined by a dielectric structure core having a first surface, the first surface including a first conducting pad having an edge (figure 2, item 18); and a second conducting pad having an edge separated from and adjacent to the edge of the first conducting pad (figure 2, item 18), the edges of the first and second conducting pads defining therebetween a surface area of the first surface (figure 2, item 20); applying a solder paste on the first and second conducting pads and on the first surface of the dielectric structure core, the solder paste at least partially covering the surface area of the first surface between the edges of the first and second conducting pads to form a substantially zero signal degradation electrical connection between the first and second conducting pads (col. 4, l. 15); further including the step of: performing reflow soldering of the solder paste applied to the

first and second conducting pads and the surface area of the first surface of the dielectric structure core (col. 4, ll. 10-30); wherein the step of applying the solder paste includes the steps of: placing a stencil on the first surface of the dielectric structure core, the stencil defining a first opening sized to substantially correspond to the first conducting pad, a second opening sized to substantially correspond to the second conducting pad and a third opening that links the first opening to the second opening and is sized to correspond to a partial portion of the surface area of the first surface between the edges of the first and second conducting pads; and applying the solder paste onto the stencil so that the solder paste flows through the first, second and third openings and onto the first and second conducting pads and the first surface of the dielectric structure core (col. 3, ll. 60-67); wherein the step of applying the solder paste includes: applying the solder paste on the first surface of the dielectric structure core such that the solder paste covers substantially all of the surface area of the first surface between the edges of the first and second conducting pads to form a substantially zero signal degradation electrical connection between the first and second conducting pads (col. 3, ll. 60-67); wherein the step of applying the solder paste includes the steps of: placing a stencil on the first surface of the dielectric structure core, the stencil defining a first opening sized to correspond to a portion of the first conducting pad, a second opening sized to correspond to a portion of the second conducting pad, and a third opening that links the first opening to the second opening and is sized to correspond to a partial portion of the surface area of the first surface of the dielectric structure core between the edges of the first and second conducting pads; and applying the solder paste onto the stencil so that the solder paste flows through the first, second, and third openings and onto the portions of the first and second conducting pads and onto the partial a portion of the surface area of the first surface

of the dielectric structure core (col. 3 ll. 60-67); removing the stencil from the first surface of the dielectric structure core; and performing reflow soldering of the solder paste applied to the first and second conducting pads and the surface area of the first surface of the dielectric structure core (col. 3, l. 60 to col. 4, l. 30); wherein the step of applying the solder paste includes the steps of: placing a stencil on the first surface of the dielectric structure core, the stencil defining an opening sized to substantially correspond to the first conducting pad, the second conducting pad and substantially the entire surface area of the first surface between the edges of the first and second conducting pads; and applying the solder paste onto the stencil so that the solder paste flows through the opening and onto the first and second conducting pads and the first surface of the dielectric structure core (col. 3, ll, 60-67); removing the stencil from the first surface of the dielectric structure core; and performing reflow soldering of the solder paste applied to the first and second conducting pads and the surface area of the first surface of the dielectric structure core (col. 4, ll. 1-25); wherein the stencil includes a plurality of openings in addition to the opening, and wherein prior to the step of placing the stencil on the first surface of the dielectric core the method includes the step of: masking off at least one opening of the plurality of openings such that the solder paste is prevented from flowing through the at least one opening (col. 3, l. 65 to col. 4, l. 10); wherein the edge of the second conducting pad is separated from the edge of the first conducting pad by a pad edge-to-pad edge separation distance of less than 8 mils (col. 4, l. 67); wherein the pad edge-to-pad edge separation distance is 8 mils (col. 4, l. 67); removing the stencil from the first surface of the dielectric structure core; and performing reflow soldering of the solder paste applied to the first and second conducting pads and the surface area of the first surface of the dielectric structure core (col. 4, ll. 1-65);

wherein the step of applying the soldering paste includes the steps of: placing a stencil on the first surface of the dielectric structure core, the stencil defining an opening sized to correspond to a portion of the first conducting pad, a portion of the second conducting pad and a portion of the surface area of the first surface of the dielectric structure core between the edges of the first and second conducting pads; and applying the solder paste onto the stencil so that the solder paste flows through the opening and onto portions of the first and second conducting pads and onto the portion of the surface area of the first surface of the dielectric structure core (col. 4, ll. 1-50); removing the stencil from the first surface of the dielectric structure core; and performing reflow soldering of the solder paste applied to the first and second conducting pads and the surface area of the first surface of the dielectric structure core (col. 4, ll. 1-50).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan Johnson whose telephone number is 571-272-1177. The examiner can normally be reached on M-Th 7:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Dunn can be reached on 571-272-1171. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jonathan Johnson
Primary Examiner
Art Unit 1725

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